CSC 203

B.Sc. IVth SEMESTER EXAMINATION, 2023-24

COMPUTER SCIENCE

(Computer System Architecture)

Credit (4+0)

(CBCS Mode)

AFFIX PRESCRIBED RUBBER STAMP

Date (तिथि) : _____

Paper ID
(To be filled in the OMR Sheet)

5377

अनुक्रमांक (अंकों में) :
Roll No. (In Figures) :

अनुक्रमांक (शब्दों में) : _____

Roll No. (In Words) : _____

Time : 1:30 Hrs.
समय : 1:30 घण्टे

Max. Marks : 75
अधिकतम अंक : 75

नोट : पुस्तिका में 50 प्रश्न दिये गये हैं, सभी प्रश्न करने होंगे। प्रत्येक प्रश्न 1.5 अंक का होगा।

Important Instructions :

1. The candidate will write his/her Roll Number only at the places provided for, i.e. on the cover page and on the OMR answer sheet at the end and nowhere else.
2. Immediately on receipt of the question booklet, the candidate should check up the booklet and ensure that it contains all the pages and that no question is missing. If the candidate finds any discrepancy in the question booklet, he/she should report the invigilator within 10 minutes of the issue of this booklet and a fresh question booklet without any discrepancy be obtained.

महत्वपूर्ण निर्देश :

1. अभ्यर्थी अपने अनुक्रमांक केवल उन्हीं स्थानों पर लिखेंगे जो इसके लिए दिये गये हैं, अर्थात् प्रश्न पुस्तिका के मुख्य पृष्ठ तथा साथ दिये गये ओ०एम०आर० उत्तर पत्र पर, तथा अन्यत्र कहीं नहीं लिखेंगे।
2. प्रश्न पुस्तिका मिलते ही अभ्यर्थी को जाँच करके सुनिश्चित कर लेना चाहिए कि इस पुस्तिका में पूरे पृष्ठ हैं और कोई प्रश्न छूटा तो नहीं है। यदि कोई विसंगति है तो प्रश्न पुस्तिका मिलने के 10 मिनट के भीतर ही कक्ष परिप्रेक्षक को सूचित करना चाहिए और बिना त्रुटि की दूसरी प्रश्न पुस्तिका प्राप्त कर लेना चाहिए।

1. What is computer architecture ?

(A) A set of categories and methods that specify the functioning, organization, and implementation of computer systems.

(B) A set of principles and methods that specify the functioning, organization, and implementation of computer systems.

(C) A set of functions and methods that specify the functioning, organization and implementation of computer systems.

(D) None of the mentioned.

2. What is computer organization?

(A) The structure and behavior of a computer system as observed by the user.

(B) The structure of a computer system as observed by the developer.

(C) The structure and behavior of a computer system as observed by the developer.

(D) None of the mentioned.

3. The instruction Add #45, R1 does _____

(A) Adds the value of 45 to the address of R1 and stores 45 in that address.

(B) Adds 45 to the value of R1 and stores it in R1.

(C) Find the memory location 45 and adds that content to that of R1.

(D) None of the mentioned

4. On addition of +38 and -20 using 2's complement, we get _____

(A) 11110001

(B) 100001110

(C) 010010

(D) 110101011

5. What is the primary purpose of a Karnaugh map (K-map)?

(A) To minimize logic expressions

(B) To maximize logic expressions

(C) To sum parity bits

(D) To create logic gates

6. In the case of the Zero-address instruction method, the operands are stored in :

(A) Registers.

(B) Accumulators.

(C) Push-down stack.

(D) Cache.

7. In memory- mapped I/O _____

(A) The I/O devices and the memory share the same address space.

(B) The I/O devices have a separate address space.

(C) The memory and I/O devices have an associated address space.

(D) A part of the memory is specifically set aside for the I/O operation.

8. Simplify the expression using K-maps : $F(A,B,C,D) = \sum(1,3,5,6,7,11,13,14)$ the result will be :

(A) AB+BC'D+A'B'C

(B) BCD'+A'C'D+BD'

(C) A'D+BCD+A'BC+AB'C'

(D) AC'D'+BC+A'BD+C'D'

9. The usual BUS structure used to connect the I/O devices is _____

(A) Star BUS structure.

(B) Multiple BUS structure.

(C) Single BUS structure.

(D) Node to Node BUS structure.

10. The advantage of I/O mapped devices over memory mapped is _____

(A) The former offers faster transfer of data.

(B) The devices connected using I/O mapping have a bigger buffer space.

(C) The devices have to deal with fewer address lines.

(D) No advantage as such.

11. The system is notified of a read or write operation by_____

(A) Appending an extra bit of the address.

(B) Enabling the reader write bits of the devices.

(C) Raising an appropriate interrupt signal.

(D) Sending a special signal along the BUS.

12. The complement of the Boolean expression (A+B). (A+C).(A+D') is :

(A) A'.(B'+C'+D)

(B) A+B.C.D

(C) A+B.C'+D'

(D) A+B+C+D

13. On Simplifying the expression using K-maps: $F(A,B,C) = \Sigma(1,3,5,6,7)$ result will be :

(A) AC'+B'

(B) AB+C

(C) AB'+B'C'

(D) A'BC+B'C+AC

14. The method of accessing I/O devices by repeatedly checking status flags is ____

(A) Program- controlled I/O.

(B) Memory-mapped I/O.

(C) I/O mapped.

(D) None of the mentioned

15. The method of synchronizing the processor with the I/O device in which the device sends a signal when it is ready is _____

(A) Exceptions.

(B) Signal handling.

(C) Interrupts.

(D) DMA.

16. On subtracting $(01010)_2$ from $(11110)_2$ using 1's complement, we get _____

(A) 01001

(B) 11010

(C) 10101

(D) 10100

17. How many select lines would be required for an 8- line-to-1-line multiplexer?

(A) 2

(B) 4

(C) 8

(D) 3

18. The method that offers higher speeds of I/O transfers is _____

(A) Interrupts.

(B) Memory mapping.

(C) Program-controlled I/O.

(D) DMA.

19. What is a multiplexer?

(A) It is a type of decoder which decodes several inputs and gives one output.

(B) A multiplexer is a device which converts many signals into one

(C) It takes one input and results into many output.

(D) It is a type of encoder which decodes several inputs and gives one output.

20. On addition of -33 and -40 using 2's complement, we get _____

(A) 1001110

(B) -110101

(C) 0110001

(D) -1001001

21. The Boolean expression X+XY will be equal to :

(A) X+Y

(B) Y

(C) X

(D) 1

22. The process where in the processor constantly checks status flags is called ____

(A) Polling.

(B) Inspection.

(C) Reviewing.

(D) Echoing.

23. NAND gate can be also expressed in :

(A) invert-OR

(B) invert-AND

(C) invert-NOT

(D) invert-NORs

24. The logic operations are implemented using _____circuits.

(A) Bridge

(B) Logical

(C) Combinatorial

(D) Gate

25. Which of the following represents the number of output lines for a decoder with 4 input lines ?

(A) 15

(B) 16

(C) 17

(D) 18

26. A digital multiplexer is a combinational circuit that selects _____

(A) One digital information from several sources and transmits the selected one

(B) Many digital information and convert them into one

(C) Many decimal inputs and transmits the selected information

(D) Many decimal outputs and accepts the selected information

27. In an S-R flip-flop, if Q = 0, the output is said to be _____

(A) Set

(B) Reset

(C) Previous state

(D) Current state

28. The logic circuits whose outputs at any instant of time depend not only on the present input but also on the past outputs are called _____

(A) Combinational circuits

(B) Sequential circuits

(C) Latches

(D) Flip-flops

29. In full adders, the sum circuit is implemented using _____

(A) AND & OR gates

(B) NAND gate

(C) XOR

(D) XNOR

30. 2's complement of 11001011 is _____

(A) 01010111

(B) 11010100

(C) 00110101

(D) 11100010

31. The usual implementation of the carry circuit involves_____

(A) AND & OR gates

(B) XOR

(C) NAND

(D) XNOR

32. Which of the following allows simultaneous write and read operations ?

(A) ROM

(B) EROM

(C) RAM

(D) None of these

33. The small, extremely fast RAMs are called_____

(A) Heaps

(B) Accumulators

(C) Stacks

(D) Cache

34. Convert the following decimal number to 8-bit binary 187:

(A) 10111011_2

(B) 11011101_2

(C) 10111101_2

(D) 10111100_2

35. Convert binary 111111110010 to hexadecimal.

(A) $EE2_{16}$

(B) $FF2_{16}$

(C) $2FE_{16}$

(D) $FD2_{16}$

36. Convert the binary number 1001.0010_2 to decimal.

(A) 90.125

(B) 9.125

(C) 125

(D) 12.5

37. Convert $8B3F_{16}$ binary

(A) 35647

(B) 011010

(C) 1011001111100011

(D) 1000101100111111

38. Convert the following octal number $(17)_8$ to decimal

(A) 51

(B) 82

(C) 57

(D) 15

39. Which one of the following is not a universal gate ?

(A) EX-NOR

(B) NAND

(C) NOR

(D) None of the above

40. If the two inputs are 00 then the OR gate output will be _____

(A) High

(B) Low

(C) Moderate

(D) Constant

41. In the toggle mode a JK flip-flop has

(A) J=0, K=0.

(B) J=1, K=1.

(C) J=0, K=1

(D) J=1, K=0.

42. A digital circuit that can store on bit is a

(A) XOR gate

(B) flip-flop

(C) gate

(D) register

43. The total number of Maxterms for four variables will be :

(A) 8

(B) 12

(C) 14

(D) 16

44. RTL stands for:

(A) Random transfer language

(B) Register transfer language

(C) Arithmetic transfer language

(D) All of these

45. The smallest square in K-map represents:

(A) Max term

(B) Min term

(C) both of these

(D) None of these

46. The register for the program counter is signified as _____:

(A) MAR

(B) PC

(C) IR

(D) None of these

47. Which mirco operations carry information from one register to another :

(A) Register transfer

(B) Arithmetic

(C) Logical

(D) All of these

48. Every transfer, selection of register by bus is decided by:

(A) Control signal

(B) No signal

(C) All signal

(D) All of above

49. Which of the following computer memory is fastest ?

(A) Register

(B) Hard Disk

(C) RAM

(D) None of these

50. Which operation refers bitwise manipulation of contents of register:

(A) Logical micro operation

(B) Arithmetic micro operation

(C) Shift micro operation

(D) None of these

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